This listing of claims will replace all prior versions, and listings, of claims in the present application.

**LISTING OF CLAIMS**:

Claim 1 (Previously Presented) A semiconductor IC structure comprising:

a semiconductor substrate including at least one front-end-of-the-line device (FEOL) located on a surface thereof;

at least one metal resistor located on, or in close proximity to, said surface of said semiconductor substrate, said at least one metal resistor comprising at least a conductive metal; and

a first level of metallization above said at least one metal resistor.

Claim 2 (Previously Presented) The semiconductor IC structure of Claim 1 further comprising a trench isolation region in said semiconductor substrate, and said at least one metal resistor is positioned on said trench isolation region.

Claim 3 (Original) The semiconductor IC structure of Claim 1 wherein said conductive metal comprises Ta, TaN, Ti, TiN, W, WN, NiCr, SiCr or a metal silicide.

Claim 5 (Original) The semiconductor IC structure of Claim 1 wherein said conductive metal has a thickness from about 20 to about 50 nm.

Claim 6 (Original) The semiconductor IC structure of Claim 1 further comprising an etch stop layer located beneath said conductive metal.

Claim 7 (Original) The semiconductor IC structure of Claim 6 wherein said etch stop layer has a thickness from about 20 to about 50 nm.

Claim 8 (Previously Presented) The semiconductor IC structure of Claim 1 further comprising a dielectric material on said at least one metal resistor.

Claim 9 (Original) The semiconductor IC structure of Claim 1 wherein said first level of metallization comprises an interlevel dielectric material having contact openings that are filled with a conductive material.

Claim 10 (Original) The semiconductor IC structure of Claim 1 wherein said at least one FEOL device comprises a field effect transistor, a bipolar transistor, a BiCMOS device, or a passive device.

Claims 11 – 40 (Cancelled)